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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/994,545	11/26/2001	Peter Rabkin	00939A-085300US	8177

20350 7590 08/29/2002

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EXAMINER

IM, JUNGHWA M

ART UNIT	PAPER NUMBER
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2811

DATE MAILED: 08/29/2002

6

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/994,545	Applicant(s) RABKIN ET AL. <i>RE</i>	
	Examiner Junghwa M. Im	Art Unit 2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 02 July 2002.
- 2a) ☐ This action is FINAL. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-35 is/are pending in the application.
- 4a) Of the above claim(s) 1-16 is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 17-35 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
 Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☐ The proposed drawing correction filed on _____ is: a) ☐ approved b) ☐ disapproved by the Examiner.
 If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

- 13) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
 a) ☐ All b) ☐ Some * c) ☐ None of:
 1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
 * See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
 a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) Paper No(s). _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Election/Restrictions

Applicant's election without traverse of claims 17-35 in Paper No. 5 is acknowledged.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 17-24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yeh et al. (U.S. Pat. No. 5,840,607) in view of Wang (U.S. Pat. No. 4,992,391).

Regarding claim 17, Yeh et al. disclose, in Fig. 4, a semiconductor non-volatile memory cell comprising;

a first insulating layer (20) on a substrate region;

a first doped polysilicon layer (24) over the first insulating layer;

a first undoped polysilicon layer (26) over and in contact with the first doped polysilicon layer, the first doped polysilicon layer and the first undoped polysilicon layer forming a floating gate;

a second insulating layer over (28, 30, 32) and in contact with the first undoped polysilicon layer; and

a second doped polysilicon layer (34) forming a control gate.

Art Unit: 2811

Yeh et al. do not show a memory device with a control gate with a second undoped polysilicon layer which is formed over and in contact with the second insulating layer.

However, Wang shows, in Fig. 5-B, a memory device with a control gate made of undoped polysilicon layers (18, 22) and a doped layer polysilicon (20) over an insulating layer (16)

It would have been obvious to one of ordinary skill in the art to combine the teachings Yeh et al. and Wang to form a two layered control gate since a second undoped polysilicon of the control gate on the insulating layer reduces oxidation rate which allows better process control of the insulating layer (ONO).

Regarding claim 18, Yeh et al. disclose, in Fig. 4, a third doped polysilicon layer (22) over and in contact with the first insulating layer (20) wherein the first doped polysilicon layer (24) overlies and is in contact with the third undoped polysilicon layer, the third undoped polysilicon layer forming a part of the floating gate (col.2, lines 18-20);

Regarding claim 19, Yeh et al. disclose that the first insulating layer (20) is a tunnel oxide (col.2, line21) and the second insulating layer is one of a composite oxide-nitride-oxide dielectric layer and a composite oxide-nitride-oxide-nitride dielectric layer (col. 2, lines 26-28).

Regarding claim 20, Yeh et al. disclose a thickness of each doped polysilicon is greater than a thickness of a corresponding undoped polysilicon layer by a factor in the range of two to four (col.3, lines 34-45).

Regarding claim 21, Yeh et al. disclose, in Fig.4, the memory cell comprising insulating spacers (42) along sidewalls of the stack made up of the first insulating layer, the floating gate, the second insulating layer, and the control gate; and

source and drain regions (44) in the substrate.

Regarding claim 22, Yeh et al. disclose that the first and second doped polysilicon layers are in-situ doped with impurities (co. 3, lines 32-36).

Regarding claim 23, Yeh et al. disclose that the memory cells any one of a stacked-gate cell and split gate cell (line 1 of Abstract).

Regarding claim 24, Yeh et al. disclose that each of the first and second doped polysilicon layers has a doping concentration and a thickness greater than a thickness of the corresponding first and second undoped polysilicon layers so as to prevent polysilicon depletion in each of the floating gate and the control gate (col.3, lines 22- 29).

Yeh et al. disclose that the formation of impurity diffusion on the doped polysilicon layer. Therefore , it can be deduced that the doped polysilicon layer has a doping concentration.

In addition, Wang also discloses that doped polysilicon layers have a doping concentration. See the respective portions of the Wang's specification.

Regarding claim 25, Yeh et al. disclose that the non-volatile cell is any one of ROM, flash EPROM, and EEPROM (col.2, line 24).

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 26, 27, 31 and 33 are rejected under 35 U.S.C. 102(b) as being anticipated

Art Unit: 2811

by Wang.

Regarding claim 26, Wang discloses, in Fig.5-B, a semiconductor transistor comprising:

- an insulating layer over a substrate region (16);
- an undoped polysilicon layer (18) over and in contact with the insulating layer; and
- a doped polysilicon layer (20) over and in contact with the undoped polysilicon layer, the doped and undoped polysilicon layers forming a gate (control gate) of the transistor.

Regarding claim 27, Wang discloses that the insulating layer is a gate oxide layer (col. 4, line 33).

Regarding claim 31, Wang discloses that the transistor is any one of an NMOS transistor, PMOS transistor, enhanced MOS transistor, and depletion MOS transistor (col.2, line 58).

Regarding claim 33, Wang discloses, in Fig.5-B, a semiconductor structure comprising:

- an undoped polysilicon layer (18);
- a doped polysilicon layer (20) in contact with the undoped polysilicon layer; and
- an insulating layer (16) in contact with the undoped polysilicon layer, wherein the undoped polysilicon layer is sandwiched between the doped polysilicon layer and the insulating layer.

Claims 26-35 are rejected under 35 U.S.C. 103(a) as being unpatentable over Wang in view of Yeh et al..

Regarding claims 26 and 33, motivation for combining two teachings has been stated above in claim 1.

Regarding claim 28, Yeh et al. disclose that a thickness of each doped polysilicon is greater than a thickness of the undoped polysilicon layer by a factor in the range of two to four (col.3, lines 34-45).

Regarding claim 29, Yeh et al. disclose, in Fig. 4, the transistor further comprising:
insulating spacers (42) along sidewalls of the gate; and
source and drain regions in the substrate.

Regarding claim 30, Yeh et al. disclose the doped polysilicon layer is in-situ doped with impurities (co. 3, lines 32-36).

Regarding claim 32, Yeh et al. disclose that the doped polysilicon layer has a doping concentration and a thickness greater than a thickness of the undoped polysilicon layer so as to prevent polysilicon depletion in the gate (col.3, lines 22- 29).

Also, see claim 24 for detailed statement.

Regarding claim 34, Yeh et al. disclose that a thickness of each doped polysilicon is greater than a thickness of the undoped polysilicon layer by a factor in the range of two to four (col.3, lines 22- 29).

Regarding claim 35, Yeh et al. disclose that the structure is one of a ROM cell, a flash EPROM cell, an EEPROM cell, a DRAM cell, a SRAM cell, a NMOS transistor, a PMOS transistor, an enhanced MOS transistor, and a depletion MOS transistor (col.2, line 24).

Art Unit: 2811

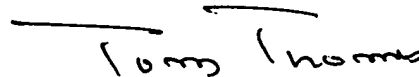
Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Junghwa M. Im whose telephone number is (703) 305-3998. The examiner can normally be reached on MON.-FRI. 8:30AM-5:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on (703) 308-2772. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 308-7722 for regular communications and (703) 308-7724 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

JMI
August 21, 2002

A handwritten signature in black ink that reads "Tom Thomas". The signature is written in a cursive style with a horizontal line above the first name.

TOM THOMAS
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800